Low power W:AlO$_x$/WO$_x$ bilayer resistive switching structure based on conductive filament formation and rupture mechanism

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We report the design and fabrication of W:AlO$_x$/WO$_x$ bilayer based resistive switching cells in a standard 0.18 μm CMOS process with only one extra mask. The devices show excellent performance with low power consumption. Low operation voltages (SET voltage < 1.5 V, RESET voltage < 1.3 V) are achieved, and specifically, the RESET and SET currents are lower than 1 μA. For the 0.3 μm $\times$ 0.3 μm active area of the cell, the current density is below 1.1×10^3 A/cm^2, which is much smaller than previous reported results. To reveal the resistive switching mechanism, various physical analysis techniques were employed to examine the microstructures, compositions, and chemical states. Current-voltage and capacitance-voltage electrical characterizations were carried out on these devices. Based on the physical and electrical characteristics, a conductive filament formation and rupture mechanism is proposed to explain the W:AlO$_x$/WO$_x$ bilayer structure resistive switching phenomena. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4803462]

As memory technologies continue scaling beyond 16 nm generation, conventional flash memory technologies have reached some major physical barriers as predicted in international technology roadmap for semiconductors (ITRS 2011). Resistive switching memory (RRAM) has been widely considered as one of the most promising candidates for next generation nonvolatile memories. Various transition metal oxides, such as NiO$_x$,[1] TiO$_x$,[2] ZrOx,[3] TaO$_x$,[4,5] and HfO$_x$,[6,7] have been investigated. RRAM process compatibility with CMOS is one of the critical requirements for RRAM mass production. WO$_x$ based RRAM is attractive because W is a standard CMOS backend material.[8] However, low initial resistance and high forming voltage are common problems in previous reported results.[9] The low initial resistance causes large current and large voltage on serially connected transistor which makes RRAM array design difficult. In order to overcome those challenges, a method to lift the initial resistance is reported by scaling down the cell size to 40 nm.[10,11]

Previous research works have shown that bilayer structure exhibits better switching performances than single layer RRAM cell[5] based on mechanism analysis.[12] The appropriately selected bilayer materials and precisely controlled thickness of each layer showed better switching uniformity,[6,13] higher cycling endurance,[4] longer retention,[5] and lower operation current.[14–16]

In this paper, a fully CMOS-compatible WO$_x$-based RRAM structure is developed. Single layer WO$_x$ and bilayer W:AlO$_x$/WO$_x$ based RRAM were fabricated, and their performances were compared. By introducing the W:AlO$_x$/WO$_x$ bilayer structure, the initial resistance shows significant increase without scaling down the device size. Here W:AlO$_x$ means certain amount W atoms exist in AlO$_x$ layer. Furthermore the RESET current could be as low as 1 μA which is corresponding to a current density of

1.1×10^3 A/cm^2, much smaller than previous reported results.[9,16,17] Detail physical analysis and electrical measurements were carried out to understand the switching mechanism.

WO$_x$ based RRAM cells are fabricated using a standard 0.18 μm CMOS process with only one extra mask in Shanghai HHNEC CMOS foundry. Figure 1(a) shows the major fabrication steps: (1) Rapid thermal oxidation (RTO) to produce WO$_x$ layer after chemical mechanical polishing (CMP) of W; (2) pattern and dry etch to clean the WO$_x$ in via regions without RRAM cells; (3) top electrode (TE) deposition, TiN/Al, or Al in this study; (4) rapid thermal annealing (RTA) process after the deposition of Al layer—this is to form W:AlO$_x$ switching layer through interdiffusion between Al and WO$_x$ layers. Figure 1(b) shows the cell structure of TiN/WO$_x$/W/Al and Al/W:AlO$_x$/WO$_x$/W/Al cells. In order to check the impact of RTA conditions on the RRAM cell performance, different RTA conditions were tested: skip RTA, 400 °C 30 s, 400 °C 50 s, and 450 °C 50 s.

To investigate the resistive switching behavior of the W:AlO$_x$/WO$_x$ bilayer RRAM cell, various analysis techniques were employed. The cell cross section structure was investigated by field-emission transmission electron microcopy (TEM, FEI TF20). The compositions and chemical states were analyzed by X-ray photoelectron spectroscopy (XPS, ESCALAB 250Xi) depth profile technique. The RRAM cell electrical performance was tested by current-voltage (I-V) and capacitance-voltage (C-V) using Agilent B1500A semiconductor parameter analyzer and 81110A pulse generator.

At the beginning, the WO$_x$ layer is formed by RTO step or by RTO plus downstream plasma oxidation (DSPO) which is similar to methods described in previous reports.[9] The single layer WO$_x$ RRAM cell has the structure of TiN/WO$_x$/W with 65 nm thick WO$_x$ layer and 0.3 μm in diameter. The 8-in. wafer level tests showed very low initial resistance (<100 Ω) of RRAM cells. Different oxidation conditions and

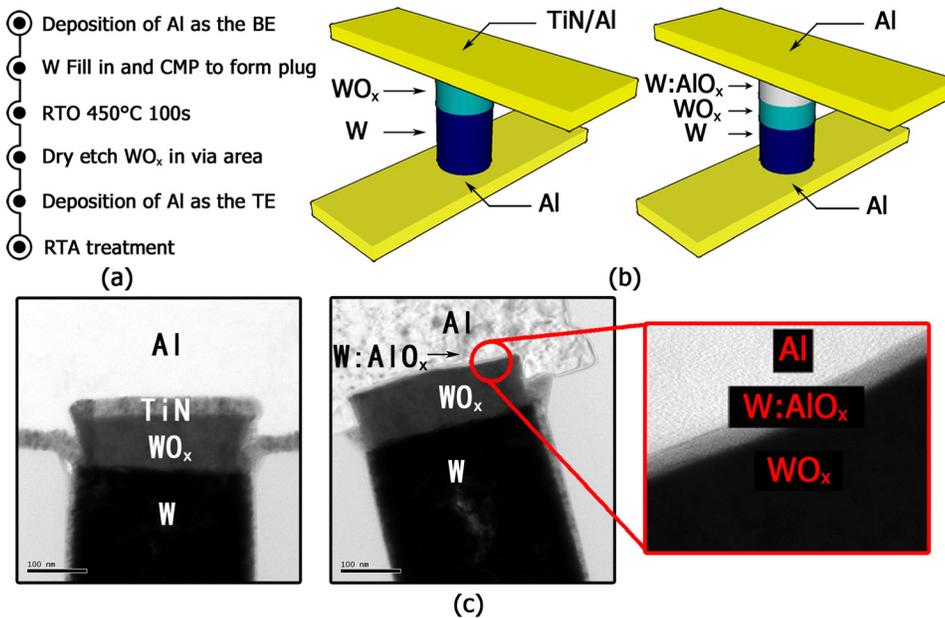[a]Author to whom correspondence should be addressed. Electronic mail: wuhq@tsinghua.edu.cn

FIG. 1. (a) Fabrication process of TiN/WO_x/W/Al and Al/W:AlO_x/WO_x/W/Al resistive switching devices with (b) schematic structures and (c) TEM cross-sectional images.

techniques (RTO/DSPO) were tried to get different thickness of WO_x and/or different composition inside WO_x layer. However, the initial resistances only change slightly with WO_x thickness, as shown in the inset of Figure 2(a). The low initial resistance of cell is due to that the majority of the WO_x layer is composed of high conductive WO_2 and W_2O_5, analyzed by XPS. Based on many round experiments, it is very difficult to significantly increase the initial resistance by changing RTO conditions. These results are similar to previous reported data,[9] where the cell initial resistances are smaller than 500 Ω. Figure 2(a) shows a typical double I-V sweeping curves for the WO_x RRAM cells. The initial resistance of this device is only 30 Ω, and the forming voltage is 10 V at 50 ns pulse width. After the forming, the device resistance increases to 25 kΩ. As shown in Figure 2(a), after the forming, the device SET voltage is −0.8 V, and RESET voltage is 1.2 V. Such low initial resistance and high forming voltage are not suitable for large RRAM arrays with 1T1R structures.

To solve the low initial resistance problem while keeping CMOS compatibility, a W:AlO_x/WO_x bilayer RRAM structure is proposed and Figure 1(a) shows the key fabrication steps. Figure 1(c) shows the cross-sectional TEM image of Al/W:AlO_x/WO_x/W devices. A bright thin layer can be observed between Al and WO_x layers, which indicates an intermediate layer is formed between Al and WO_x due to interdiffusion. The thickness of W:AlO_x layer could be controlled through RTA conditions.

Wafer level measurements showed much higher initial resistance, 100 kΩ–10 MΩ, of W:AlO_x/WO_x bilayer RRAM cell. Inset image of Figure 2(b) shows the average initial resistance from four 8-in. wafers with different RTA treatment conditions. As expected, stronger RTA conditions produce thicker W:AlO_x layer which results in larger initial resistance. This strong correlation provides a method to control the cell initial resistance without changing cell size.

Figure 2(b) shows the measurement results of double DC I-V sweeping from −1.5 V to 2 V on RRAM cells. The W:AlO_x/WO_x bilayer devices show the reverse switching

polarity in comparison to single layer WO_x devices. When the applied SET voltage scanned from 0 V to 2 V, a threshold voltage for resistance switching from high resistive state (HRS) to low resistive state (LRS) was observed at 1.2 V. Similarly, the RESET voltage scanned from 0 V to −1.5 V, a decline of current was observed around −1.2 V. For W:AlO_x/WO_x bilayer devices, the first SET sweeping step is considered as the forming operation. Differing from very large forming voltage in single layer WO_x RRAM devices, the forming step I-V curve is almost the same as the following SET operation I-V curves which means the bilayer RRAM cells have forming free property. Moreover the W:AlO_x/WO_x bilayer cells show the low power operation property. The RESET current is as low as 1 μA with 1 μA current compliance during SET operation. Since the cell active area is 0.3 μm × 0.3 μm, the RESET current density is only 1.1×10^3 A/cm^2 which is 1–3 orders lower than previous reported results (3.4×10^6, 6.2×10^4, 8×10^5 A/cm^2).[9,16,17]

Good endurance property is achieved by balanced SET/RESET pulse cycling operations on W:AlO_x/WO_x bilayer RRAM cells. As Figure 3(a) shows that the cells have stable cycling with 10 kΩ and 1 kΩ for HRS and LRS, respectively.
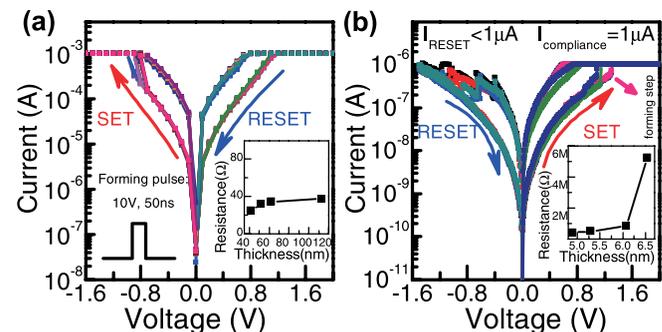

FIG. 2. Typical double I-V sweeping of (a) single layer WO_x RRAM devices with 10 V/50 ns forming pulse and (b) W:AlO_x/WO_x bilayer RRAM devices with 1 μA current compliance. Inset images show the initial resistance distribution with (a) different thicknesses of WO_x layers and (b) different thicknesses of W:AlO_x layers.

Figure 3(b) shows read retention tests on W:AlO$_x$/WO$_x$ RRAM cells. Using 0.1 V read voltage with 10 ms pulse width, the HRS and LRS did not show any destruction after 10^5 times of read cycles. Those endurance and retention testing results showed excellent cell performance.

To further understand the W:AlO$_x$/WO$_x$ bilayer structure, the XPS depth profile scans were used with monochromatic Al Kα (1486.6 eV) radiation. The absolute binding energy scale was calibrated by adjusting the C 1s peak at 284.8 eV. Figure 4(a) shows the atomic percentage by fitting O 1s, Al 2p, and W 4f peaks. The concentration of O rises after 2000 s etching time and declines after 4000 s, which indicates an existence of oxygen-rich layer. In order to distinguish this oxide layer, O 1s peaks were analyzed as shown in Figure 4(b). Four points (2200 s, 4200 s, 6200 s, and 7800 s etching time) with distinct compositions were chosen for analysis. The O 1s spectra at the points 1 and 4 show a singlet peak at 532.1 ± 0.5 eV and 530.8 ± 0.5 eV which correlate to AlO$_x$ and WO$_x$ seperately.[18] The O 1s peaks at points 2 and 3 are the combination of these two peaks. Curve-fitting results show that the ratio of area between these two peaks is 70:30 at point 2 and 36:64 at point 3, which confirm the oxide layer transformed from AlO$_x$ to WO$_x$. Figures 4(c) and 4(d) show Al 2p and W 4f peaks with chemical valence states of each element. A combination of two singlet peaks at 75.1 ± 0.5 eV and 72 ± 0.5 eV correlated to AlO$_x$ and Al.[19] The Al metal component is the highest at the surface and the AlO$_x$ reaches the highest around point 2. W 4f peak is the doublet peak with 4f$_{7/2}$-4f$_{5/2}$ spin-orbit splitting of 2.15 eV. The spectra are fitting with three doublet peaks with W 4f$_{7/2}$ peak at 31.4 ± 0.2 eV, 32.2 ± 0.2 eV, and 35.6 ± 0.2 eV correlated to three chemical state W^{0+}, W^{4+}, and W^{6+} of tungsten.[20] As observed from the XPS results, few tungsten atoms are in the form of WO$_3$. The whole WO$_x$ layer is mainly composed of WO$_2$ and W. Figure 4(e) shows the overall XPS analysis results where the etching time was converted into physical depth calibrated with surface profilometer (Veeco Dektak 150). The Al dominated layer is 87 nm thick below the surface corresponding to the top Al layer thickness after polishing removal of most Al layer. The W:AlO$_x$ with W intermediate layer is 6.4 nm thick, and WO$_x$ layer is 53 nm thick which agrees with TEM observations very well.

Previous works have shown that single WO layer exhibits opposite switching directions by changing WO$_x$ thickness from 15 nm to 160 nm.[21] In this study, the opposite switching
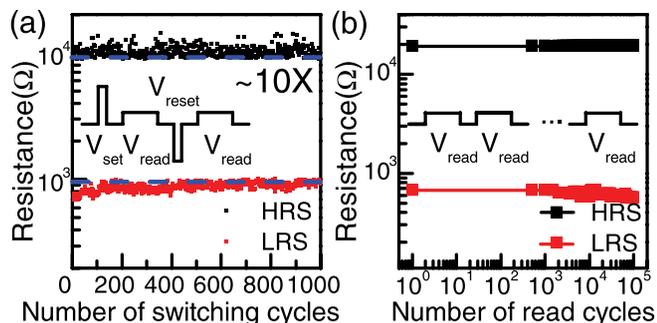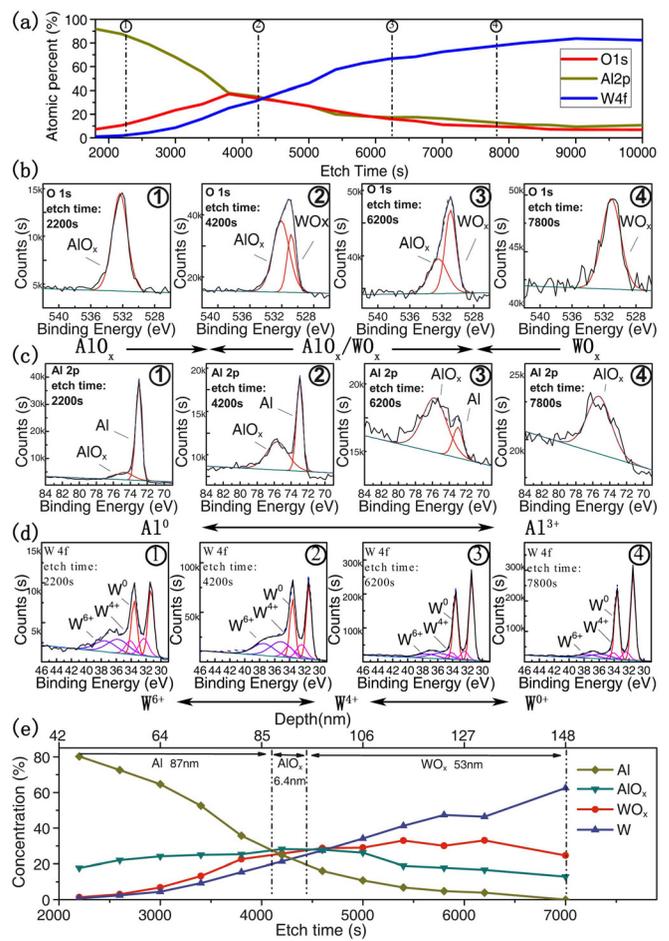

FIG. 4. (a) XPS depth profile of Al/W:AlO$_x$/WO$_x$/W/Al stack. According to (b) O 1s, (c) Al 2p, and (d) W 4f XPS spectra, the concentration is summarized in (e).

polarity is due to bilayer structure and different TE. Based on physical and electrical analysis results, one possible switching mechanism is shown in Figure 5. In single WO$_x$ layer devices with TiN TE, most of W is in the form of W, WO$_2$, and W$_2$O$_5$ which are all high conductive. When a high positive forming voltage (10 V) is applied on the TiN, reduction reactions occur, and oxygen ions move to the interface of TiN and WO$_x$ layers. Due to the oxygen blocking role played by TiN, the oxygen ions cannot drift into TiN TE and accumulate near the TiN/WOx interface.[9] It is possible that, across a thin top WO$_x$ layer, oxygen ions combine with WO$_x$ and form a continuous WO$_3$ layer which gives the whole cell high resistance state. During the next SET operation, with a negative voltage applied on TiN TE, at some locations, oxygen ions move out of WO$_3$ layer and form an oxygen vacancy conductive path. However, for W:AlO$_x$/WO$_x$ bilayer case, a high resistance layer of W:AlO$_x$ is already formed due to inter-diffusion between Al and WO$_x$ layers under RTA treatment. When positive voltage is applied on Al TE, oxygen ions move out of WO$_x$ or AlO$_x$ (most probably WO$_x$ since W-O has weaker bond strength in comparison to Al-O bond). In some preferred locations, such as grain boundaries or defect locations, conductive filament (CF) could be formed. Those oxygen ions diffused to Al TE could react with top Al electrode. However, oxygen ions could diffuse to a large surrounding three dimensional volume under density
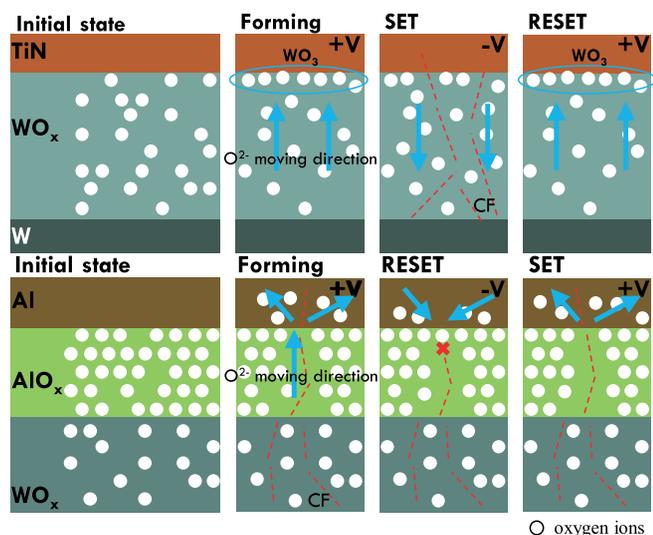

FIG. 3. (a) Pulse cycles of Al/W:AlO$_x$/WO$_x$ bilayer RRAM devices, (b) data retention characteristics with 0.1 V/10 ms read pulse.

FIG. 5. Schematics of resistive switching mechanism of TiN/WO$_x$/W/Al and Al/W:AlO$_x$/WO$_x$/W/Al devices in initial state, forming, SET and RESET process.

gradient, assisted by high temperature around CF. Al electrode on top of the CF is only partially oxidized and does not block the whole CF. When negative voltage is applied on top Al electrode, the oxygen ions move back to CF, which break the conductive path and bring the cell back to high resistance value. The following SET/REST happens on the CF formation and rupture process in W:AlO$_x$ layer.

In summary, A fully CMOS compatible W:AlO$_x$/WO$_x$ bilayer RRAM structure was designed and developed. The W:AlO$_x$ layer is formed by the inter-diffusion between Al and WO$_x$ layer under RTA treatment. By controlling the RTA conditions, the cell initial resistance could be made larger than 10 MΩ. This type of RRAM cells are forming free and suitable for large RRAM array. Low power operations on those cells are demonstrated as V$_{set}$ < 1.5 V, V$_{reset}$ < 1.3 V, and both SET and RESET currents are below 1 μA. The forming free and low power operations are excellent characteristics for future nonvolatile memories with high storage capacity. Physical and electrical analysis indicates that CF formation and rupture is a possible mechanism for cell switching.

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